AMENDMENTS TO THE CLAIMS

1. (Currently amended) Signal delaying device [[(1)]] for the dynamic delaying of a digitally sampled input signal with a memory element [[(2)]] and a series connected interpolation element [[(3)]], ~~wherein,~~ comprising a register ~~(30), which can be connected to the~~ that has its output side [[of]] connected to the input side of the interpolation element [[(3)]] for the intermediate storage of at least one sampled value ($S_{in}(k)$) of the input signal[[,]] and is arranged in parallel to the memory element [[(2)]], and a marking device which, after a sampled value ($S_{in}(k)$) of the input signal has been placed in intermediate storage in the register, adds a marking to the next sampled value ($S_{in}(k+1)$) of the input signal stored in the memory element.

2. (Canceled)

3. (Currently amended) Signal delaying device according to claim [[2]] 1, characterized in that the interpolation element [[(3)]] checks whether the marking has arrived at the output of the memory element [[(2)]], and following this, reads out a sampled value (x(k)) from the memory element [[(2)]] and also a sampled value from the register [[(30)]].

4. (Currently amended) ~~Signal delaying device according to any one of claims 1-3, characterized in that~~ Signal delaying device for the dynamic delaying of a digitally sampled input signal with a memory element and a series connected interpolation element, comprising a register having its output side connected to the input side of the interpolation element for the intermediate storage of at least one sampled value ($S_{in}(k)$) of the input signal and arranged in parallel to the memory element, wherein the interpolation element [[(3)]] comprises a polyphase filter [[(5)]].

5. (Currently amended) Signal delaying device according to claim 4, ~~characterized in that~~ wherein the interpolation element [[(3)]] comprises a half-band filter [[(4)]], which is arranged between the memory element [[(2)]] and the register on one side, and the polyphase filter on the other side.

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6. (Currently amended) Method for the dynamic delaying of a digitally sampled input signal with the following procedural stages:

- ~~storage of the~~ storing sampled values of the input signal in a memory element [[(2)]],
- reading out of the sampled values ($S_{in}(k)$) from the memory element [[(2)]],
- ~~interpolation of~~ interpolating the sampled values (x(k)) read out from the memory element [[(2)]], wherein
- whenever the range [[(19)]] defined by two successive sampled values (x(k-4), x(k-3)) is neither undercut nor exceeded in the interpolation, one sampled value ($S_{in}(k)$) is placed into the memory element [[(2)]] and one sampled value (x(k)) is read out from the memory element [[(2)]],
- whenever the range [[(20)]] defined by two successive sampled values (x(k-4), x(k-3)) is exceeded in the interpolation, no new sampled value (x(k)) is read out from the memory element [[(2)]],
- before the range [[(21)]] defined by two successive sampled values (x(k-4), x(k-3)) is undercut in the interpolation, placing a sampled value ($S_{in}(k)$) of the input signal ~~is placed~~ in intermediate storage in a register [[(30)]] arranged in parallel to the memory element [[(2)]], marking the next sampled value ($S_{in}(k+1)$) of the input signal stored in the memory element [[(2)]] ~~is marked~~, and reading out a sampled value from the memory element [[(2)]] and also the sampled value placed in intermediate storage in the register [[(30)]] ~~are read out~~, whenever the marked sampled value arrives at the output of the memory element [[(2)]].

7. (Currently amended) Method according to claim 6, ~~characterized in that~~ wherein the range [[(20)]] defined by two successive sampled values (x(k-4), x(k-3)) is exceeded, if at least two interpolation values ($S_{out}(k-3)$, $S_{out}(k-2)$) produced by the interpolation fall within this range [[(20)]].

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8. (Currently amended) Method according to claim 6 or 7, ~~characterized in that~~ wherein the range [[(21)]] defined by two successive sampled values (x(k-4), x(k-3)) is undercut in the interpolation, if no interpolation value produced by the interpolation falls within this range.

9. (Currently amended) Method according to any one of claims 6-7, ~~characterized in that~~ wherein storage in the memory element [[(2)]] takes place by means of a write pointer, and reading out from the memory element [[(2)]] takes place by means of a read pointer, wherein the write pointer and the read pointer in each case point towards a given memory cell of the memory element,

wherein the write pointer and also the read pointer are adjusted if the range [[(19)]] defined by two successive sampled values (x(k-4), x(k-3)) is neither undercut nor exceeded in the interpolation.

10. (Currently amended) Method according to claim 9, ~~characterized in that~~ wherein only the write pointer but not the read pointer is adjusted, if the range [[(20)]] defined by two successive sampled values (x(k-4), x(k-3)) is exceeded in the interpolation.

11. (Currently amended) Method according to claim 9 ~~characterized in that,~~ wherein only the read pointer but not the write pointer is adjusted, if a sampled value is stored in the register [[(30)]].

12. (Currently amended) Method according to claim 9, ~~characterized in that~~ wherein both the write pointer and also the read pointer are adjusted, if a sampled value is read out from the register [[(30)]].

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